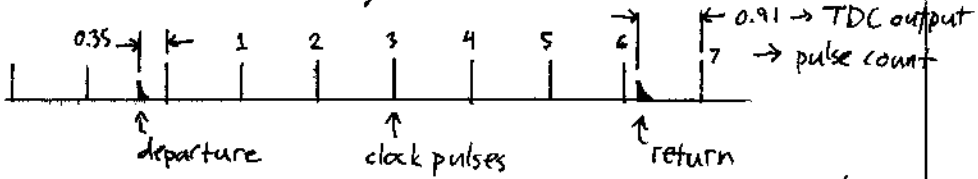
APOLLO Timing/Control Scheme

Zeroth Order

- Measure round trip travel time of photon bouncing off moon (reflector).

First Order

- Use APDs to generate temporally reliable detection events.
- Place corner-cube in exit beam to generate "departure" signal.
- Measure time interval between departure and return signals
  - Combination of counting clock pulses and fractional intervals



In this example, $\Delta T = 7 + 0.35 - 0.91 = 6.44$ clock periods

Second Order

- Know time of laser fire to $< 1\mu s$ UTC (via GPS clock)
- Compute distance to moon for each pulse launched
- Adjust mirror rate to put departure & return signals ~180° out of phase → maximum breathing room (> 20 ms)
- Use computed moon distance to tell 100ns APD gate when to open
- Employ many-bit counters to keep track of important time intervals:

Fiducial Times:

Fast Photodiode STOP clock pulse	: PINST
Calibration gate ON clock pulse	: CALON
Calibration gate OFF clock pulse	: CALOFF
Lunar gate ON clock pulse	: LUNON
Lunar gate OFF clock pulse	: LUNOFF

Counters:

PPS (Pulse per second) counter: reset by GPS clock, latched on CALOFF, LUNOFF
↳ where within second did gate OFF occur?

CPS (counts per second) counter: reset by GPS PPS, latched by GPS PPS
↳ sanity check: how many clock pulses per second?

FRC (free-running counter): never reset, latched by CALOFF, LUNOFF
↳ provides uninterrupted continuity; basis "language" for lunar delay (LUNON)

GWC (gate width counter): reset by CALON, LUNON; controls gate duration

CAL (calibrator) gate delay: reset by fast photodiode; controls CALON

PIN (PIN photodiode): reset by photodiode, latched by CALOFF, LUNOFF
↳ keeps track of laser fire-to-departure signal clock pulses

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Second Order (cont.)

- TDCs (Time-to Digital Converters) precisely measure short intervals (< 100 ns) to 25 ps resolution. TDCs measure time between photon signal and fiducial clock pulse. Phillips Scientific 7186H has 16 TDC channels.
- Computer retrieves TDC data (via CAMAC) and latched counter values every ~25 ms.
- Counter/Comparator/Latch configuration programmed into humongous Programmable Logic Device.
- Fast photodiode in laser housing serves as high signal-to-noise alert of the beginning of the cycle. The CFD (constant fraction discriminator)-triggered leading edge is timed relative to the master clock by a TDC channel

Discussion on:

- General scheme / Approach
- Implementation
- Test version for lab work
- Data I/O